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S-I-S mm-WAVE MIXERS AND DETECTORS

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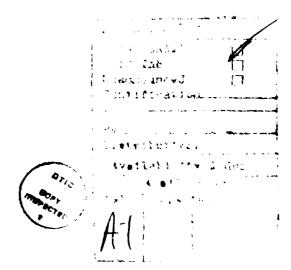
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This program is an effort to achieve the ultimate goal of fabricating refractory superconducting S-I-S mixer devices for operation in mm-wave receivers in the quantum mode and in the 8-10 K temperature range. The following progress has been made toward the above goal: (1) development of in-house capability of depositing niobium carbonitride films (NbC _x N _y) of device quality with transition temperatures to ~16 K; (2) development of NbC _x N _y :aSi:Nb and NbC _x N _y :Ge:Nb devices of very high quality; (3) fabrication and successful operation of niobium based S-I-S				
mixer chips; and (4) fabrication and evaluation of aSi and Ge barrier all-NbC $_{ m x}$ N $_{ m y}$ devices.				

SECURITY CLASSIFICATION OF THIS PAGE(When Date Entered) NbC_xN_y:Ge:Nb devices have been fabricated with chemical vapor deposited (CVD) polycrystalline arsenic-doped germanium barriers. The figures of merit for these junctions are: $J_o \sim 80\text{--}200 \text{ A/cm}^2$, $I_o R = 2.2 \text{ mV}$, $V_g = 3.95 \text{ mV}$, $\Delta V_g = 0.1 \text{ mV}$ and $V_m \lesssim 48 \text{ mV}$. NbC_xN_y:aSi:Nb devices using a composite silicon barrier have been developed to yield $J_o \sim 1.00$ 80-500, I_0R = 1.9 mV, V_g = 4.1 mV, ΔV_g = 0.4 mV and $V_m \lesssim$ 70 mV. These excellent results indicate that both barriers are suitable candidates for devices fabricated with NbC_xN_y counterelectrodes. All-Nb S-I-S mixer chips were fabricated and sent to Goddard Institute for Space Studies to be evaluated. The noise temperature was ~ 60 K and the conversion loss of 5 dB. These results are comparable to Pb alloy junction results. A second-generation mixer was designed by GISS.

TABLE OF CONTENTS

Section		Page
1	INTRODUCTION	1
2	NbC _x N _y DEPOSITION	3
3	DEVICE RESULTS	9
	3.1 NbC _x N _y /aSi/Nb Devices	9
	3.2 NbC _x N _y /Ge/Nb Devices	12
	3.3 All-NbC _x N _y Devices	12
4	MIXER RESULTS	16
5	CONCLUSIONS	17
6	REFERENCES	18
7	APPENDIX	19



LIST OF ILLUSTRATIONS

Figure		Page
1	A schematic diagram of the system used at SRC to deposit NbC_XN_Y films. The ion pumps are typically valved off and not used	4
2	The transition temperature as a function of methane partial pressure of NbC _x N _y films deposited at NRL "ambient" conditions (actually 425°C), SRC ambient conditions, and SRC heated (200°C) conditions.	7
3	A high quality NbC_xN_y -aSi:H-Nb device using NRL supplied NbC_xN_y	11
4	A companion device to Fig. 3 fabricated using SRC deposited NbC _x N _y	13
	LIST OF TABLES	
Table		Page
1	Parameters for deposition of the best NbC_xN_y (\sim 16 K T_c) films in SRC's system	6

SECTION 1 INTRODUCTION

The work performed under NRL Contract No. N00014-81-C-2525 Mod. No. P00001 is described in this report. This work is an ongoing effort to develop all-refractory, high $T_{\rm C}$ mm-wave mixers operating at 8-10 K. Although this goal remains for the future, very significant progress has been made. Previous related work has been performed under NRL Contract No. N00173-80-0159, completed in September 1981; and N00014-81-C-2525, completed in September 1982.

The superconductor chosen as the basis of this work is NbC_xN_v . This material is reactive sputter deposited, which results in the Bl (rock salt) NbN structure in which carbon plays a significant rule in stabilizing the deposited film in this desired structure. The best films have $T_c \sim 16 \text{ K}$, which is sufficient for device operation at $8-10~\mathrm{K}$. The majority of the NbC_yN_y used in this work was deposited at NRL by Dr. E. Cukauskas [1,2], and the vast majority of development work on these films was completed by Dr. Cukauskas. However, in order to expedite device development it was necessary to have an in-house source of $NbC_{\chi}N_{\chi}$, rather than continuing the shipping of wafers back and forth between SRC and NRL. Thus, during the previous contract an existing UHV system was adapted for NbC,N, depositions, and initial characterization runs were completed [3]. The best result obtained at that time was $T_c \sim 13.5$ K. The optical reflectivity was rather low, < 70 percent at $\lambda = 850$ nm, indicating poor quality in terms of potential device applications. This was corroborated by fabricating two of the best wafers into junctions using the aSi barrier and Nb counterelectrodes. The best devices were of S-I-S character, but with extremely large leakage currents.

During the previous contract a number of improvements were made in developing NbC $_{\rm X}$ N $_{\rm y}$ /aSi/Nb devices. These devices are a useful stepping stone towards developing all-NbC $_{\rm X}$ N $_{\rm y}$ devices. As a result of our ongoing Nb work the aSi/Nb upper interface/barrier combination is already very well controlled and of high quality. Thus attention can be focused on improving

the quality of the NbC $_{\rm X}$ N $_{\rm y}$ /aSi lower interface/barrier combination. It was found that using a low power sputter etch of the NbC $_{\rm X}$ N $_{\rm y}$ lower electrode resulted in increased I $_{\rm o}$ R and V $_{\rm g}$ due to reduced damage of the surface during sputter etching. In addition, the composite barrier that was found to be successful in reducing subgap leakage in all-Nb junctions was equally successful in reducing subgap leakage in NbC $_{\rm X}$ N $_{\rm y}$ /Nb junctions. Also during the previous contract some fabrications of all-NbC $_{\rm X}$ N $_{\rm y}$ junctions using the aSi barrier and the thermal oxidation variant of SNAP were done. The best result was junctions with a definite S-I-S character, but with a reduced gap and very high subgap leakage.

During this period, S-I-S mm-wave mixers were designed with the help of personnel at the Goddard Institute for Space Studies (GISS). Fabrication had begun, but no mixer chips had been completed and evaluated.

Significant progress has been made over the past year in all the areas reported above. In the next section, deposition of high $T_{\rm C}$, device quality, ${\rm NbC_XN_y}$ films is described. Section 3 covers all Josephson device results. Of particular significance is the development of a chemical vapor deposited germanium barrier. This barrier was initially developed on ${\rm NbC_XN_y}/{\rm Nb}$ junctions. Since the barrier is grown at $380^{\circ}{\rm C}$ it should be more stable than the Si barrier under high temperatures. This is important because the potential best ${\rm NbC_XN_y}$ counterelectrodes will probably have to be deposited onto a heated surface.

Section 4 covers S-I-S mm-wave mixer results. First generation chips were fabricated and evaluated at GISS, giving good performance. A second generation chip has been designed, but masks have not yet been procured for it. The last section concludes this report with some thoughts on remaining problems in the satisfaction of the overall goal of producing useful mm-wave detectors operating at 8-10 K.

$\begin{array}{c} \text{SECTION 2} \\ \text{NbC}_{\mathbf{X}} \mathbf{N}_{\mathbf{y}} \text{ DEPOSITION} \end{array}$

The evaluation of superconducting thin films \underline{per} \underline{se} is usually made by T_c , X-ray diffraction, resistivity, composition (typically using Auger electron spectroscopy), and residual resistance ratio. For our purposes, the most important aspect of film quality is the electrical characteristics of tunnel junctions fabricated using the film. Low leakage S-I-S tunnel junctions with a very sharp rise at the superconducting energy gap are essential for successful S-I-S mm-wave mixers that can operate in the quantum limit.

All the NbC $_{\rm X}$ N $_{\rm y}$ used in this effort prior to this report was deposited by Dr. E. Cukauskas at NRL. By all the measures of film quality mentioned above, including device quality, this material is excellent. Also, as the relevant conditions affecting the film quality have come to be understood, the reproducibility of the NRL films has improved. The major problem with this arrangement has been the time required to ship wafers between NRL and SRC. In addition, wafers are subject to increased contamination and breakage or loss during shipping. In order to shorten the total time required to fabricate NbC $_{\rm X}$ N $_{\rm y}$ devices, and to expedite progress in fabricating all-NbC $_{\rm X}$ N $_{\rm y}$ devices SRC decided, during the previous contract, to develop an independent NbC $_{\rm X}$ N $_{\rm y}$ deposition capability.

An existing ion-pumped UHV system was adapted for NbC_xN_y deposition. This system is shown schematically in Fig. 1. It is equipped with an 8" diameter niobium target and a 500 W rf power supply. The anode table can be heated. However, maximum heater power is not available for more than 15 minutes due to heating of the elastomer seals in the J-arm. A CTI CT-8 cryopump has been installed directly adjacent to the chamber. The ion pumps are normally valved off during operation.

The first ${\rm NbC}_{\rm X}{\rm N}_{\rm y}$ films were made using no anode heating. This was an attempt to emulate NRL results for ambient temperature depositions.

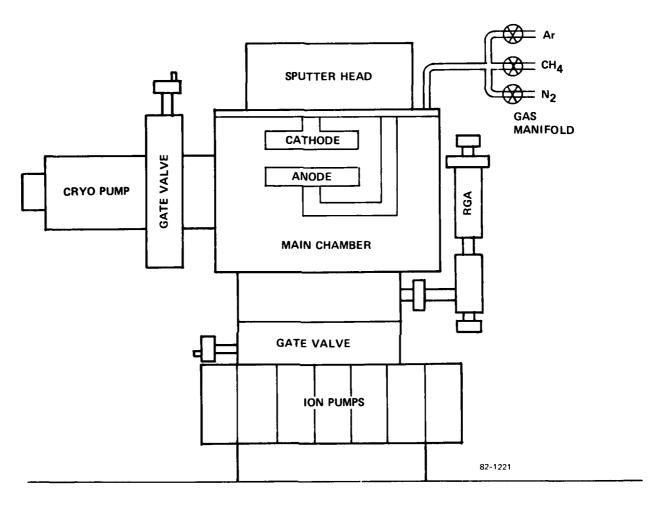


FIG. 1 A schematic diagram of the system used at SRC to deposit $NbC_{\chi}N_{\chi}$ films. The ion pumps are typically valved off and not used.

It was subsequently found that the NRL "ambient" temperature was 425°C due to high rf power (1.5 kW) applied to a smaller 6" diameter cathode. Their best films deposited at this temperature had $T_{\rm C}=15.6$ K. Our best results were $T_{\rm C}\sim13.5$ K. Also, the quality of junctions fabricated using our films was very poor, whereas NRL's ambient films yielded very good devices.

Since a larger rf power supply was not available, it was not possible to duplicate NRL conditions directly. Instead, the anode was heated to 200°C during deposition. This amount of heat could be sustained indefinitely by the system. The system parameters that produce the best films are indicated in Table I. These films typically have $T_{\text{C}} \sim 16~\text{K}$ and can be used to produce Josephson devices having low leakage and good overall quality. The NRL films are still slightly superior in terms of device quality, but the SRC films are more than adequate for device development. It is expected that the use of increased anode heat will yield better films. This improvement requires the installation of water cooling on the J-arm feedthrough.

The dependence of transition temperature on methane partial pressure is shown in Fig. 2 for SRC films deposited at ambient and at 200°C anode temperature. Also shown is the NRL "ambient" result, actually 425°C as mentioned above. The transition temperature at zero $\mathrm{CH_4}$ partial pressure can fluctuate drastically, depending on the partial pressure of hydrocarbons in the system during deposition. This depends on system history. Typically, $\mathrm{T_C}$ will go down on successive depositions made with no methane as the system gradually "cleans" itself. Since the SRC and NRL systems are quite different, and different deposition parameters are used, the two results are not directly comparable. Nonetheless, it appears that there is a broad maximum in $\mathrm{T_C}$ at appropriate $\mathrm{CH_4}$ pressures. Also, at higher substrate temperatures less $\mathrm{CH_4}$ pressure is required to achieve high $\mathrm{T_C}$ films.

A few of the SRC films have been examined by Auger electron spectroscopy. The Auger system was not accurately calibrated. However, the best films show relatively large amounts of carbon. Our estimates would indicate a composition of Nb $_2$ CN. This is consistent with NRL's result of NbC $_{0.4}$ N $_{0.6}$ for their best "ambient" films. The role the carbon plays in

Ar	CH ₄	N ₂	Time	Power	Heating
Pressure	Pressure	Pressure			
9.24 μ	.05 μ	.71 µ	30 Min	500 W	200° C Minimum

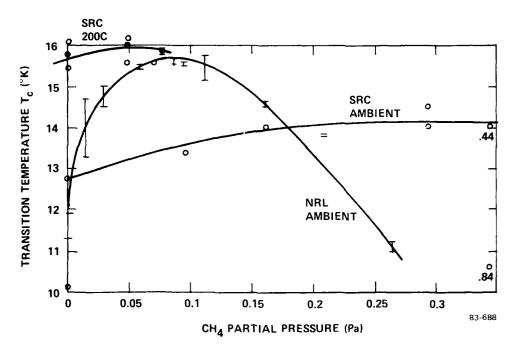


FIG. 2 The transition temperature as a function of methane partial pressure of NbC_xN_y films deposited at NRL "ambient" conditions (actually 425°C), SRC ambient conditions, and SRC heated (200°C) conditions.

these films is not completely clear at this time. X-ray diffraction results indicate a mixed (111) and (200) orientation, with lattice parameter consistent with the fcc Bl structure. Given that the ratio of (C + N)/Nb is about 1 for all the better films it is reasonable to assume that carbon simply replaces the nitrogen in the Bl structure.

Optical reflectivity data from 200 nm to 900 nm wavelength are routinely taken on all our films. The rationale for this procedure is that optical reflectivity only probes the surface to a depth of several atomic layers in a metal. This is quite close to the depth probed by tunneling, which is a coherence length, \mathbb{S}_0 . \mathbb{S}_0 is presumably some tens of angstroms in our films. The reasoning behind this reflectivity rationale is reflected in the excellent correlation we have observed between reflectivity at 850 nm and the quality of the tunneling characteristic of junctions fabricated from those films [4]. The optical reflectivity at 850 nm also correlates very well with the transition temperature. The very best junctions are fabricated on $\mathsf{NbC}_{\mathsf{X}}\mathsf{N}_{\mathsf{Y}}$ samples having reflectivity > 85 percent at 850 nm.

SECTION 3 DEVICE RESULTS

There are three distinct Josephson device types that have been fabricated under this contract. Two consist of NbC $_{\rm X}$ N $_{\rm y}$ lower electrodes and Nb counterelectrodes and use either the composite sputtered aSi barrier, or an n type CVD Ge barrier. The other category of devices are those using NbC $_{\rm X}$ N $_{\rm y}$ for both electrodes, which is our ultimate goal. The NbC $_{\rm X}$ N $_{\rm y}$ /Nb devices are viewed as a useful subgoal in fabricating all-NbC $_{\rm x}$ N $_{\rm y}$ devices. Since SRC has extensive experience with all-Nb devices, it is possible to concentrate on the improvement of the lower electrode and barrier. This objective has been realized, and excellent quality Josephson junctions with the NbC $_{\rm x}$ N $_{\rm y}$ /Nb structure have been fabricated using both the aSi and the Ge barrier. Recent activity has thus centered on the problem of fabricating devices with these barriers and having NbC $_{\rm x}$ N $_{\rm y}$ counterelectrodes. This section of the report will discuss these three major device types separately.

3.1 $NbC_xN_y/aSi/Nb$ Devices

Under previous NRL contract support this device type had already been developed to a fairly high level [3]. It had been found that a lower power sputter etch resulted in improved $I_{\rm O}R$ and $V_{\rm g}$. Previously sputter etches were done at 500 W for 5 minutes, the new technique used a 20 W sputter etch for a full hour. In the interest of saving time this has been changed to 100 W for 5 minutes without any deterioration in device quality. It is fairly certain that the Ar bombardment during high power sputter etching amorphotizes the NbC $_{\rm X}N_{\rm y}$ surface to deeper levels. The Japanese group at Ibaraki found that this amorphous layer [5] led to a poor less dense oxide in the tunneling barrier. In our case, the tunneling barrier is deposited aSi (or CVD Ge) so that the deterioration may be due to degradation of the NbC $_{\rm X}N_{\rm y}$ material next to the barrier.

The other improvement previously made was the use of the composite barrier that was originally developed on all-Nb junctions. This barrier

consists of a thin aSi layer, followed by a thicker hydrogenated aSi layer (aSi:H) and then another thin unhydrogenated aSi layer. The purpose of the two unhydrogenated asi layers is to prevent the hydrogenated layer from "poisoning" the niobium electrodes. It is not clear that hydrogen would "poison" ${
m NbC}_{
m x}{
m N}_{
m v}$ (especially since ${
m NbC}_{
m x}{
m N}_{
m v}$ is deposited in a ${
m CH}_4$ partial pressure); nonetheless, for purposes of comparison and expediency, this composite barrier (aSi/aSi:H/aSi) was carried over to the NbC $_{\rm X}$ N $_{\rm V}$ /Nb structure. The thickness of the aSi:H was reduced to 3/4 that used for all-Nb junctions in order to compensate for the increased barrier height of the NbC_vN_v/aSi interface [3]. Otherwise the same procedure was used. Typically the aSi/aSi:H/aSi depositions are done for 15 seconds, 45 seconds and 15 seconds respectively at a V_{csb} of 640 volts, which results in a power of ~ 100 watts. The depositions are done at a pressure of 8 mT Ar, to which a partial pressure of 0.5 mT $\rm H_2$ is added for the hydrogenated layer. All barriers receive a 150°C 1/2 hour 0_2 thermal treatment before being reinserted into the vacuum system for the Nb counterelectrode deposition. Niobium counterelectrode deposition and device completion using the SNAP process are identical to previously published techniques used for all-Nb devices.

The composite barrier yielded the same results on both NbC $_{\rm X}$ N $_{\rm y}$ and Nb base electrodes: The I $_{\rm O}$ R product increased and subgap leakage decreased dramatically. What was not done under the previous contract was to combine the lower power sputter etch with the composite barrier. This has now been done, and the result combines the improvements noted for both of those process modifications. An I-V curve is shown in Fig. 3. The relevant device parameters are: I $_{\rm O}$ R = 1.9 mV, V $_{\rm m}$ = 70 mV, V $_{\rm g}$ = 3.8 mV and $_{\rm W}$ V $_{\rm g}$ = 0.4 mV in a current density range of 50-700 A. The base electrode was NN294, deposited at NRL. This film had very high reflectivity, R = 88 percent at 850 nm. It is interesting that this film was unusual in having two NbN phases present, as evidenced by the X-ray diffraction results. This did not affect I $_{\rm O}$ R or V $_{\rm m}$, both of which are excellent, but it is possible that $_{\rm O}$ V $_{\rm g}$, which is relatively large, was affected. Further systematic study will be needed to resolve this point. The available quality in these junctions is suitable for any application requiring a tunnel junction.

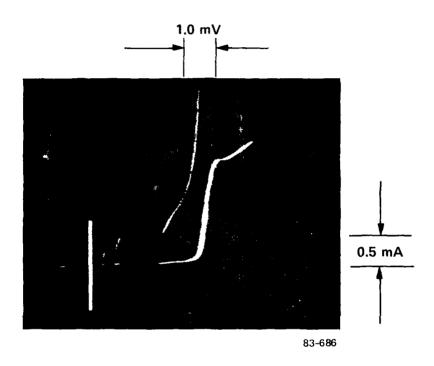


FIG. 3 A high quality NbC_xN_y -aSi:H-Nb device using NRL supplied NbC_xN_y .

Figure 4 is a device fabricated from SRC deposited $NbC_\chi N_\chi$. The barrier and counterelectrode were deposited in the same run as the device of Fig. 3, illustrating how the characteristics can vary with base electrode material.

3.2 NbC_xN_y/Ge/Nb Devices

The results on this device type have been written up for submission to Applied Physics Letters. This preprint has been included as the Appendix of this report.

3.3 All-NbC $_{x}N_{y}$ Devices

The fabrication of high quality Josephson tunnel junctions having both electrodes of ${\rm NbC}_{\rm X}{\rm N}_{\rm y}$ is the ultimate goal of this work, and also the major challenge. The problem is that the counterelectrode material within a coherence length of the barrier is most important in determining the quality of the junction, and for high $T_{\rm C}$ compound superconductors the first few monolayers deposited typically are of poorer quality (lower T_c , higher resistivity, etc.) than the upper layers of the film. NbN is perhaps the most forgiving of the compound superconductors in this regard; and the Japanese have succeeded in producing all-NbN junction of fair, but not good, quality using a native oxide barrier (they claim that their films contain little or no carbon, and can thus be truly labeled NbN) [5,6]. They found that the best junctions resulted when the substrate was at ambient temperature for the counterelectrode deposition. Raising the substrate temperature, which is generally necessary to produce higher quality NbN, resulted in reduced gap and I_oR. They blamed this on interdiffusion between the oxide barrier and the electrodes. This example points out the quandry in fabricating junctions with compound superconductor counterelectrodes: The high temperatures necessary to produce quality superconducting material are likely to speed processes that result in deterioration of the relatively thin and fragile barrier and the desired sharp/clean interfaces between the barrier and the electrodes.

Another source of heating comes about from our desire to use SNAP

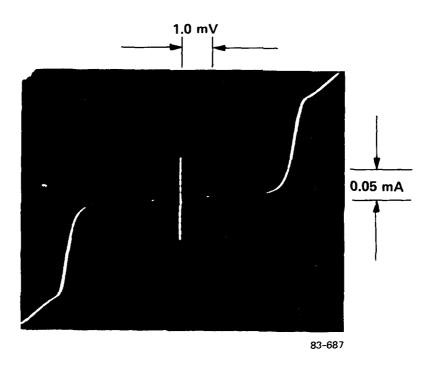


FIG. 4 A companion device to Fig. 3 fabricated using SRC deposited NbC_xN_y .

type processing for junction isolation. The advantages of doing this are two: First, the barrier is formed on a clean, unpatterned, uncontaminated surface and in principle should be more uniform, reproducible and of higher quality; and second, the same integrated circuit process developed at SRC for all-Nb junctions can be applied to ${\rm NbC}_{\chi}{\rm N}_{\chi}$ junctions. An integrated circuit process is required by the goal of S-I-S mm-wave mixer fabrication. Ideally, one could simply use anodization to isolate junctions, exactly as in Nb SNAP. The problem is that NbC_xN_y does not form a smooth insulating anodic oxide for voltages over ~ 5 V. We have done numerous experiments varying the anodization rate, solution and temperature with the same negative result. Hence, as an alternative procedure for junction isolation we have used thermal oxidation (which requires an SiO_2 mask). Annealing the $\mathrm{NbC_{x}N_{v}}$ trilayers at 400°C for 30 minutes is sufficient to convert the entire NbC_xN_v counterelectrode (typically 600 A thick) to thermal oxide. This procedure works quite well, and offers good resolution; but even if the NbC_vN_v counterelectrode can be deposited at low temperature, the sample still has to be subjected to a relatively high temperature for junction isolation.

One clue to the resistance of a given barrier to heating can be gained by annealing junctions at elevated temperatures and looking for changes in the electrical characteristics. For our all-Nb junctions with the plain asi barrier the critical current becomes larger when annealed for $\sim 1/2$ hour at 200°C. At lower temperatures they are stable. For the composite barrier the comparable temperature is 150° C. Similar behavior is exhibited by NbC $_{\rm X}N_{\rm y}/{\rm Nb}$ junctions with the same barriers. It can be postulated that the presence of a NbC $_{\rm X}N_{\rm y}$ counterelectrode would yield a more stable junction than the Nb counterelectrode due to the greater chemical stability of NbC $_{\rm X}N_{\rm y}$ (inferred from annealing NbC $_{\rm X}N_{\rm y}$ films coated with SiO $_{\rm Z}$, Si and Ge at high temperatures and looking for changes). It is equally reasonable to infer a breakdown of the barrier itself and/or the superconductor/barrier interfaces.

During the previous year of this contract a NbC $_{\rm X}$ N $_{\rm y}$ /aSi/NbC $_{\rm X}$ N $_{\rm y}$ junction with a Nb wiring layer, and with S-I-S tunneling characteristics was

fabricated. The gap voltage was very low, ~ 3 mV, and the subgap leakage was very large; but the fact that it was definitely S-I-S was taken as encouraging evidence that the aSi (noncomposite barrier) can at least partially survive the 400°C thermal oxidation (the counterelectrode was done at "ambient" temperature at NRL, ~ 425 °C). This result has not yet been reproduced, although a few attempts have been made.

One possible confound in the above device is that an inadvertent junction could be formed between the top surface of the NbC $_{\rm X}$ N $_{\rm y}$ counterelectrode and the subsequent niobium wiring layer. To check on this a NbC $_{\rm X}$ N $_{\rm y}$ sample was processed with no tunneling barrier. The desired result, superconducting shorts, was ob .rved.

Due to the fact that the CVD Ge barrier is deposited at 380°C , it can be postulated that it might be more temperature resistant than a barrier formed at lower temperatures. Attempts were made to complete devices of this structure, but insufficient time was available. It is our opinion that this structure represents the best possibility for fabricating all-NbC_xN_y junctions with very high quality tunneling characteristics.

SECTION 4 MIXER RESULTS

All-niobium S-I-S mixer chips designed at GISS have been successfully fabricated and tested. The fabrication is identical to our logic fabrication process [7] with the exception that no resistors are used. Testing was done at GISS. The chips supplied were lower resistance than desired, and also had higher leakage than our "best" junctions. Nonetheless, GISS observed a noise temperature of 60 K and a conversion loss of 5 dB. They consider these results fully comparable to their results with Pb-alloy junctions.

GISS also found that a major source of conversion loss (~ 2 dB) was due to the Cr-Au choke structures they have been using. We have recently delivered to GISS choke structures fabricated from niobium, with small gold pads in the bonding areas.

GISS has developed a second generation mixer design which uses a series capacitance and inductance to shunt the junction detector array. They expect much broader bandwidth coupling of the rf to the mixer with this design, and consequently improved performance. This design has been digitized at SRC but masks have not been fabricated.

SECTION 5 CONCLUSIONS

Excellent progress has been made on all aspects of this project except one: The fabrication of all-NbC $_{\rm x}$ N $_{\rm y}$ junctions of good electrical quality using integrated circuit compatible fabrication techniques. As discussed in the section on all-NbC $_{\rm x}$ N $_{\rm y}$ devices there are fundamental reasons why this is a difficult problem. The problem is not intractable, as demonstrated by our poor quality S-I-S result, NRL results [8] and the Japanese results [5,6]. Not all the above results are IC compatible, but they demonstrate that the basic problem of junction fabrication can be overcome.

Although the production of good quality NbC_xN_y appears to be in hand, the quality is evaluated in terms of the suitability of the material for base electrodes. It is quite possible that as future work on all- NbC_xN_y devices continues, the deposition parameters for NbC_xN_y will have to be adjusted in different ways to produce high quality for the counterelectrode.

SECTION 6 REFERENCES

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SECTION 7 APPENDIX

JOSEPHSON TUNNEL JUNCTIONS WITH CHEMICALLY VAPOR DEPOSITED POLYCRYSTALLINE GERMANIUM BARRIERS

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Naval Research Laboratory

Abstract

High quality Josephson tunnel junctions have been fabricated whose tunneling barrier is polycrystalline germanium chemically vapor deposited on a NbN base electrode and covered by a Nb counterelectrode. These junctions have excellent characteristics for device applications: values of $V_{\rm m}$ (measured at 2 mV and 4.2 K) ranging between 35–48 mV; ideal threshold curves; a steep current rise at the gap voltage; and current densities in the vicinity of 1000 A/cm².

This letter reports the fabrication of high-quality Josephson tunnel junctions whose tunnel barrier is a chemically vapor deposited (CVD) polycrystalline layer. The lower electrode is niobium nitride deposited by reactive sputter deposition, which has recently been described in detail. The barrier is germanium deposited by pyrolysis of germane at 380°C in a room pressure reactor. The upper electrode is niobium deposited by dc-magnetron sputtering. The mutual isolation of devices is obtained by the selective niobium anodization process (SNAP).

The NbN films used in these experiments are deposited at the Naval Research Laboratory and are given a low power sputter cleaning in argon at Sperry Research Center just before the wafer is introduced into the CVD reactor. 4

The germanium layers are deposited in a conventional, cold wall, horizontal flow CVD reactor whose operation (heating, introduction of gases, etc.) is automatically sequenced. The substrate is placed on a graphite susceptor which is inductively heated and the wafer is brought up to the deposition temperature in a pure argon atmosphere. The premixed gases which are introduced for film growth are argon, germane and arsine for the devices described here. Total flow is 55 cm³/min, with 3.6 percent of the flow being GeH₄ and 0.027 percent being AsH₃.

The deposition time of these barrier layers was about two minutes. We estimate the thickness to be 30-60 A based upon the growth rates and

thickness measurements of thicker films. The large uncertainty in the barrier thickness arises from a suspicion that the initial growth rate is smaller than the limiting growth rate ($\sim 25-30$ A/min) obtained for thick (> 0.1 µm) layers.

Following the deposition of the polygermanium layer, the layers are exposed to an 0_2 atmosphere at 400°C for 20 minutes. This is a precautionary step taken to oxidize the base electrode through pinholes in the barrier, and the (unconfirmed) possibility that such pinholes exist. No visual change in the barrier takes place during the oxidation treatment. Immediately before the Nb counterelectrode is deposited, the barrier is cleaned by sputter etching at a low applied power using the same techniques as previously described. 5,6

We infer from examination of thicker layers (0.5 – 2.0 μ m) that the germanium films are crystalline. X-ray diffraction shows that the films have a mixed (110) and (111) orientation. The magnitude of the room temperature resistivity is less than 1 Ω -cm, which is considerably lower than one would expect for amorphous germanium. Also the resistivity of these layers initially decreases as the temperature is lowered below room temperature, which would not be expected for amorphous materials. These n-type layers are not degenerately doped and become bulk insulators at 4.2 K.

We observed a slower growth rate of both germanium and silicon with the addition of either phosphine or arsine to produce n-type layers; a similar reduction in growth rate of CVD amorphous n-type silicon has been observed by Taniguchi et al.⁷ The slower growth rate, rather than the n-type doping, may be more important for practical considerations since the thickness of a more slowly grown layer should be more easily controlled.

Figure 1 displays the current-voltage characteristics of a 10 μ m x 10 μ m square device at 4.2 K. The critical current density J_C is ~ 560 A/cm². The superconducting energy gaps are 2.65 mV for the NbN electrode and 1.35 mV for the Nb electrode. The differential resistance at zero bias of the quasiparticle characteristic is ~ 100 times that of the normal resistance of these devices. The V_m parameter (product of I_C and the subgap resistance measured at 2 mV) is 41 mV for this particular device. The range of observed V_m on this wafer was from 35-48 mV. The product of I_C and the normal resistance is 1.8 mV. The jump in the quasiparticle current is relatively abrupt, with the change from 30 percent to 80 percent of the full gap current spanning approximately 50 μ V.

Figure 2 displays the threshold curve obtained from another device whose $J_c \sim 1100~\text{A/cm}^2$. Note that under even a four-fold expansion of the current scale the minima are close to zero. Moreover, the ratios of the heights of the secondary maxima to the zeroth order maximum are as expected for a $|\sin x/x|$ curve to within experimental accuracy. (We estimate that the Josephson penetration length is comparable to the device dimensions.) This indicates that the Josephson current density is extremely uniform over the entire area of the device. This is a comforting observation since the

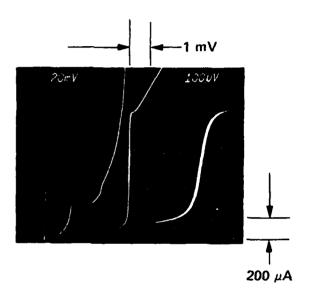


FIG. 1 I-V characteristics of a NbN-polygermanium-Nb at 4.2 K. Also shown at 10 times expansions of the current and voltage scales to show more clearly the subgap current and jump in current at the gap, respectively. (The origin of the 10 times expanded voltage trace is not on the figure.)

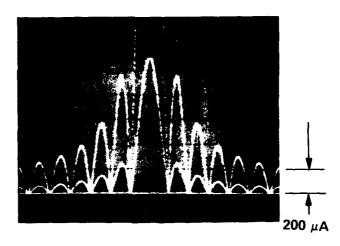


FIG. 2 Threshold curve (I_C vs. applied magnetic field) of a companion device. Also shown is a four times expansion of the current. Threshold curve is almost exactly a |sin x/x| function.

discrete grains of a polycrystalline film could result in poorer thickness uniformity than an amorphous layer. We assume that the uniformity implies a very small grain size.

We have fabricated similar structures with a CVD polycrystalline Sibarrier. These devices had fairly good threshold curves but large subgap leakage currents. We are not certain whether the superior results obtained with the germanium barriers are intrinsic to this material or if this merely reflects evolution in technique or quality of the NbN base electrode material. We have previously observed that the device quality of NbN-a5i-Nb junctions is extremely sensitive to the quality of the NbN, especially its transition temperature $T_{\rm C}$ and its optical reflectivity at 850 nm. 4 ,8

We have also fabricated devices with degenerately doped p-type Ge layers which resulted in both Josephson and super-Schottky barrier devices, qualitatively similar to those fabricated by Huang and Van Duzer on degenerately boron-doped single crystal silicon membranes. 10 The behavior of our p⁺ Ge barrier devices will be more fully described in subsequent publications.

The use of niobium nitride as a base electrode, rather than niobium, is crucial to the successful fabrication of this type of device structure, because Nb reacts with the barrier at the elevated temperatures required for the CVD of both Ge and Si. 11 We observed that reactions between Si and Nb occur not only for CV deposited Si, but also when attempting to crystallize

amorphous silicon layers previously deposited on niobium. At about 300°C, a blue layer forms whose color does not appear to be related to interference and a disruption of the Si-Nb interface is observed. On the other hand, CVD layers of Si and Ge deposited on NbN substrates do not show any obvious signs of reaction even at temperatures as high as 800°C and 600°C, respectively. 12

In summary we have described the fabrication and the electrical characteristics of NbN-cGe-Nb Josephson tunnel junctions whose barrier is deposited by chemical vapor deposition. While these characteristics are easily good enough for many digital and S-I-S mixer applications it may not be the quality of the devices which is most significant. (Indeed, these structures are not the "best" we have ever fabricated.) Rather, it may be that the method of barrier deposition is more important. The many person-years invested in developing chemical vapor depositions for the semiconductor industry could be further exploited to improve the manufacturability of these devices. Finally, because of the high deposition temperature, it may be possible to use thermal oxidation to isolate an upper niobium nitride electrode in a variation of SNAP previously suggested, 3 without risking disruption of the barrier.

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